AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

1-12. (Cancelled)

13. (Currently amended): A method of fabricating a circuit substrate, said circuit substrate having any of a passive element and an interconnection pattern, said passive element comprising at least one of a dielectric film, a resistance film and a conductor film, said method comprising a film forming step,

said film forming step forming at least one of said dielectric film, said resistance film and said conductor film by ejecting dry aerosol of a fine solid particle material together with a carrier gas.

14. (Original): The method as claimed in claim 13, wherein said circuit substrate includes a base substrate and an insulation layer laminated on said base substrate,

at least one of said base substrate and said insulation layer comprises a resin material.

15. (Original): The method as claimed in claim 13, wherein said aerosol is ejected with a velocity in the range of 3 – 400 m/second.

16. (Original): The method as claimed in claim 13, wherein said carrier gas comprises at least one of a helium gas, a neon gas, an argon gas and a nitrogen gas.

17. (Original): The method as claimed in claim 13, wherein said fine particle material comprises fine particles having an average diameter of 10nm – 1μm.

18. (Original): The method as claimed in claim 13, wherein said resin material comprises at least one of an epoxy resin, a polyimide resin, a polyester resin, a fluorocarbon copolymer, and a fiber glass.

19. (Original): The method as claimed in claim 13, further comprising a planarizing step for planarizing a surface of any of said dielectric film, resistance film and conductor film after said film forming step.

20-46. (Cancelled)

47. (Currently amended): A fabrication method of a circuit substrate in which an interlayer insulation film and a conductor layer are laminated, comprising the steps of:

forming said interlayer insulation film by spraying dry aerosol of a fine solid particle material together with a carrier gas; and

forming said conductor layer while depositing a metal or an alloy thereon.

48. (Original): The method as claimed in claim 47, wherein said step of forming said conductor layer is conducted by using any of a non-electrolytic plating process, an electrolytic plating process, a sputtering process, a vacuum evaporation deposition process and a CVD process

49. (Currently amended): The method as claimed in claim 47, further comprising the step of forming [[an]] a connection hole in said interlayer insulation film by using a hydrofluoric acid while masking said interlayer insulation film.

50. (New): A method of fabricating a circuit substrate, said circuit substrate having any of a passive element and an interconnection pattern, said passive element comprising at least one

of a dielectric film, a resistance film and a conductor film, said method comprising a film forming step,

said film forming step forming at least one of said dielectric film, said resistance film and said conductor film by impact activation of a fine solid particle material sprayed with a carrier gas in the form of aerosol.

51. (New): A fabrication method of a circuit substrate in which an interlayer insulation film and a conductor layer are laminated, comprising the steps of:

forming said interlayer insulation film by impact activation of a fine solid particle material [together] sprayed with a carrier gas in the form of aerosol; and

forming said conductor layer while depositing a metal or an alloy thereon.